

Amendment Dated Aug. 4, 2003; Reply to Office action of Jun. 19, 2003

**REMARKS/ARGUMENTS**

Examiner Yoha is thanked for her thorough examination of the subject Patent Application. The Claims have been have been carefully reviewed, several Claims have been amended in response to the Examiner's kind comments, and all Claims are now considered to be in condition for Allowance.

In the amended Figure 6, the previously omitted floating gate has been added to the schematic.

Reconsideration of the rejection of Claims 1-39 under 35 U.S.B. 102(b) as being anticipated by Ratnakumar (U.S. Patent No. 6,114,724), is requested, in light of the following.

Claims were amended to more clearly differentiate the present invention from Ratnakumar

In the present invention the source and drains of the nonvolatile memory device and the access device have the same implant profile, impurity concentration and junction depth. The method of programming the nonvolatile memory device is through a channel program operation, which means that electrons are attracted to the floating

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voltage of the memory device. The method of erasing the floating gate is through a channel erase operation, which means that electrons are expelled from the floating gate. The channel erase operation reduces the threshold voltage of the memory device. Punch through is not an issue with the present invention since erase and program operations take place between the floating gate and the channel of the memory device. Since punch through is not an issue and since the drains and sources of the memory cell (both for the nonvolatile device and the access device) are made with the same implant profile, impurity concentration and junction depth, then the size of the memory cell is determined by the read operation, which allows a smaller cell than might otherwise be possible.

Ratnakumar, on the other hand, uses an edge operation to program and erase the nonvolatile portion the two-transistor memory cell. This means that in Ratnakumar electrons are added to or removed from the floating gate of the storage device with respect to the drain. Ratnakumar discusses graded junctions and implanting on an angle to reduce leakage into the substrate, which is an issue when using edge operations. Punch through is an issue with Ratnakumar and limits the cell size (column 4, line 63 to column 5, line 3).

Ratnakumar is not the same as the present invention, does not define a shallow junction and discusses both a graded junction as well as angle implantation. Ratnakumar does not produce a symmetrical memory cell in which the size of the cell is limited by characteristics of a read operation as suggested by the Examiner but instead

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We have reviewed the related art references made of record and not relied upon and agree with the Examiner that none of these suggest the present detailed claimed invention.

All Claims are now considered to be in condition for allowance.

Allowance of all Claims is Requested.

It is requested that should Examiner Yoha not find that the Claims are now allowable, that he call the undersigned at (845) 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,  
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Attachments